First Real-Time Coherent MIMO-DSP for Six Coupled Mode Transmission

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Abstract—We present the first real-time transmission experiment over a 60-km-long fiber supporting six coupled spatial and polarization modes, enabled by a custom receiver board and an FPGA-implementation of an unconstrained adaptive frequency-domain MIMO equalizer.

I. INTRODUCTION

Today, fiber-optic communication links bridging more than a few kilometers are solely based on single-mode fibers (SMFs). Due to rapidly increasing traffic demands, more and more of these fibers are operated close to their capacity limit. This has stimulated various research efforts on novel higher-capacity fibers including fibers with multiple nominally uncoupled cores as well as fibers supporting more than two coupled spatial and polarization modes [1]. Examples for the latter are coupled-core fibers [2] (CCFs) and few-mode fibers [3], [4], [5] (FMFs) supporting propagation of multiple mode groups with different levels of coupling within and between these groups [6]. Recently, linear adaptive multiple-input multiple-output (MIMO) equalization at the receiver has been demonstrated to be effective in compensating this mode coupling, potentially increasing the fiber capacity proportionally to the number of spatial modes [3]. So far, these demonstrations have always been based on so-called offline digital signal processing (DSP), where limited-length waveforms are captured in memory and processed on a workstation. In view of real system deployments, however, the MIMO equalizer has to run in real-time and it has to be demonstrated that the system is long-term stable providing low-outage probabilities. In this work, we present the first real-time receiver for a 6×6 coupled-mode transmission channel.

II. EXPERIMENTAL SETUP AND REAL-TIME DSP

The experimental setup of our coherent-optical 6×6 MIMO system is depicted in Fig. 1a. Using a programmable-pattern generator (PPG), we generate twelve 2.5-Gb/s transmit signals modulated with 1/16-th pattern length delay-decorrelated copies of a pseudo-random binary sequence of length 2^31 − 1. Using three polarization-diversity Lithium-Niobate inphase-quadrature modulators (PD-IQMs), these signals are modulated onto an optical carrier at 1550 nm, generated from a single external cavity laser (ECL) with 100-kHz linewidth. Next, the resulting polarization-division multiplexed quadrature-phase-shift keying (PDM-QPSK) signals are amplified using three Erbium-doped fiber amplifiers (EDFAs) and the desired launch power is adjusted using three variable optical attenuators (VOAs), before the signals are launched into the three inputs of a custom photonic lantern [7] (PL) that is used as a space-division multiplexer to orthogonally launch into the 3 cores of a 60-km-long CCF [2] with a core-pitch of 29 µm and a cross-section shown in Fig. 1b. At the receiver, we first demultiplex the coupled cores using a second PL, amplify the received signals using another set of EDFAs, and detect them using three polarization-diversity integrated coherent receivers (ICRs) and a shared local oscillator ECL with 100-kHz linewidth.

In order to be able to implement the MIMO DSP in real-time, we designed and built a 28-layer printed circuit board (see Fig. 1c) which differentially connects the ICR outputs to twelve 5-G/s 10-bit SiGe analog-to-digital converters (ADCs, E2V EV10AQ190). These are interfaced to a single field-programmable gate array (FPGA, Xilinx XC7V2000T) through 480 parallel lanes running at 1.25 Gb/s each, resulting in an aggregate interface rate of 600 Gb/s. In Fig. 1d, we show the schematic of our real-time receiver DSP which we implemented in VHDL. In the schematic, each arrow represents a bus of complex numbers whose width is indicated by subscripts where relevant. Our design reads the output of each ADC with a bus width of 64 at a clock rate of 78.125 MHz. In our equalizer design, we interpret the twofold oversampling of the received signals as an additional MIMO dimension and re-partition them into twelve symbol-spaced signals each with a bus width of 32. In order to manage implementation complexity, we implement a frequency-domain equalizer using an overlap-save scheme with 50% overlap based on a split-radix 64-point fast Fourier transform (FFT) [8]. We adapt the equalizer with the constant modulus algorithm (CMA) and update one quarter of the coefficients within each clock cycle. Using an unconstrained implementation, we do not restrict the length of the equalizer to less than the FFT size, but tolerate a certain level of interference due to the cyclic property of the FFT. Previously, we have shown [9] that this can significantly reduce implementation complexity at small performance penalties. The carrier recovery consists of a frequency recovery followed by Viterbi-Viterbi phase recovery.

III. RESULTS

We tested the performance of our real-time transmission system in several steps. First, we loaded a simplified real-
time 2×1 MIMO receiver design into the FPGA and verified error-free performance on all of the 3 single-mode transmitter-receiver pairs individually. In order to test the simultaneous and properly synchronized data transfer from all 12 ADCs into the FPGA, we then connected the CCF as shown in Fig. 1a and operated the FPGA as a 12-channel real-time oscilloscope, letting it capture 12×2×18-samples-long waveforms. We then performed offline 6×6 MIMO DSP using a similar architecture to our VHDL implementation and observed error-free performance. In a further step, we loaded the FPGA with the full MIMO design as shown in Fig. 1d, increasing its overall logic utilization from ∼40% to ∼80%. In order to test the design under static channel conditions, we replaced the CCF by a 3×3 single-mode coupler, which produces static yet fully unitary coupling between the 6 spatial and polarization modes. Using this test system, we observed a bit-error-ratio (BER) of 1.5×10⁻³. We attribute this relatively high error floor to the much increased FPGA load, as we observed a significant amount of glitches in the outputs of the ADCs, indicative of clock drift in the communication between the ADCs and the FPGA, a problem that we will address and hope to eliminate in future work. Finally, we applied the 6-mode real-time MIMO receiver to the 6 signals received from the 60-km CCF, with a launch power into each fiber core of 3 dBm. In order to select each of the 6 spatial and polarization modes at the receiver, we started convergence of our real-time equalizer based on a single transmit signal and gradually increased the number of transmit signals until all 6 spatial and polarization modes were switched on. We measured the BER after differential decoding over a time frame of 30 minutes for each of the 6 spatial and polarization modes. The results are shown in Fig. 1e. As expected, we see an error floor attributed to the clock glitches above described due to the significant FPGA load, but otherwise observe stable behavior, with the 6 BERs drifting between 8×10⁻⁴ and 7×10⁻³. Exemplary constellations for all 6 recovered QPSK signals are shown in Fig. 1f.

In conclusion, we have presented the first real-time transmission experiment in which mode coupling between spatial modes in an optical fiber is compensated using an adaptive MIMO equalizer.

REFERENCES